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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,250	02/25/2004	Richard P. Schubert	A0312.70518US00	2714
7590 Edmund J. Walsh Wolf, Greenfield & Sacks, P.C. 600 Atlantic Avenue Boston, MA 02210			EXAMINER WALTER, CRAIG E	
			ART UNIT 2188	PAPER NUMBER
			MAIL DATE 11/28/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/786,250

Applicant(s)

SCHUBERT, RICHARD P.

Examiner

Craig E. Walter

Art Unit

2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 July 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 and 31-38 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18, 31-38 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application
- ☐ Other: _____

DETAILED ACTION

Status of Claims

1. Claims 1-18 and 31-38 are pending in the Application.

Claims 31-38 are new.

Claims 19-30 are cancelled.

Claims 1, 2, 4-11, 13 and 15 are amended.

Claims 1-18 and 31-38 are rejected.

Response to Amendment

2. Applicant's amendments and arguments filed on 31 July 2007 in response to the Office action mailed on 18 January 2007 have been fully considered, but they are not persuasive. Therefore, the rejections made in the previous Office action are maintained, and restated below, with changes as needed to address the amendments.

Claim Objections

3. Claims 32-34 and 37 are objected to because of the following informalities:

As for claims 32-34 and 37, it appears Applicant intended each of these claims to depend on claim 31 rather than claim 32 as presently recited. The claims will be treated on their merits based on this assumption.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 5-7 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Zangenehpour (US Patent 5,224,217).

As for claim 1, Zangenehpour teaches a method of operating a cache in a digital computer system, the cache having a plurality of memory locations, the method comprising:

a) storing a new item, the new item having an address associated therewith (data is stored in a cache based on an LRU replacement mechanism – col. 2, lines 46-58 – the location which stores the entry (i.e. item) in the cache is the address associated with that particular item), the storing comprising:

i) associating a priority with the new item based on the address associated with the item (col. 3, lines 23-44 – all memory locations are assigned a priority tag ranging from 0 to the total number of locations.

When a replacement is made, the lowest priority is identified, and replaced first. Since the address of the item to be replaced is identified and assigned a priority, the priority is associated with that new item “based on the address associated with the item” (i.e. the address was identified to be

the LRU entry, therefore the priority assigned at that location will be of higher priority once the new entry is written)).

ii) selecting a memory location in the cache based in part on priority indicators of the plurality of memory locations in the cache relative to the priority of the new item (col. 3, lines 23-44 – lowest priority item is the first to be replaced); and

iii) storing the new item in the selected memory location (col. 3, lines 23-44 – the newest entry is stored in the location from which the lowest priority item was recently purged); and

b) associating the priority associated with the new item with the selected memory location in the cache (col. 3, lines 23-44 – again, highest priority is assigned to the newest entry).

As for claim 5, Zangenehpour teaches wherein selecting a memory location in the cache based in part on the priority indicators comprises:

a) when the cache has an empty memory location suitable for storing the new item, storing the new item in an empty memory location (data needed is cached until the cache is full, then entries are replaced); and

b) when the cache has no empty memory location suitable for storing the new item and there is no least recently used (LRU) memory location with a priority indicator that is the same or lower than the new item, not storing the new item and treating the new item as not cacheable (col. 3, lines 23-44 – Zangenehpour teaches assigning the highest priority to the newest item, and

decrementing the priority of all other entries. In other words, once the cache is full, there will always be a lower priority remaining in the cache relative to the others. Additionally note in col. 3, lines 27-28 – the lowest priority item is replaced first. Zangenehpour's system ensures that only lower priority items are overwritten by higher priority ones, therefore the item would not be cacheable as recited in Applicant's claims should all the items in the cache be the same or of higher priority).

As for claim 6, Zangenehpour teaches wherein selecting a memory location in the cache based in part on the priority indicators comprises: storing the new item in the least recently used memory location with a priority indicator that is the same or lower than the new item, if one exists (col. 3, lines 23-44 – the newest entry is stored in the location from which the lowest priority item was recently purged).

As for claim 7, Zangenehpour teaches wherein selecting a memory location in the cache based in part on the priority indicators comprises: storing the new item in the least recently used memory location with a priority indicator that is lower than the new item, if one exists (col. 3, lines 23-44 – the newest entry is stored in the location from which the lowest priority item was recently purged).

As for claim 12, Zangenehpour teaches the cache contains a data array and a tag array and associating a priority indicator with a memory location comprises storing a value in a field in the tag array (Fig. 2 – each cache frame contains data (element 32), and a tag (element 31), which contains the priority field - col. 4, lines 5-18).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 17, 18, 31, 32 and 34, 35, 37, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zangenehpour (US Patent 5,224,217) and in further view of Abe et al. (US Patent 5,906,000), hereinafter Abe.

As for claim 31, Zangenehpour teaches a method of operating a cache in a digital computer system, the cache having a plurality of memory locations, the method comprising:

a) identifying a plurality of blocks of addresses in memory of the computer system and a priority associated with each of the plurality of blocks of memory (col. 3, lines 23-44 – all memory locations of a cache are assigned a priority tag ranging from 0 to the total number of locations);

b) receiving an item having an address associated therewith (each item received inherently must have an address associated with it);

c) obtaining a priority associated with a block of the plurality of blocks of addresses containing the address associated with the item (col. 3, lines 23-44 – when a replacement is made, the lowest priority is identified, and replaced first. Since the address of the item to be replaced is identified and assigned a priority, the priority is

associated with that new item "based on the address associated with the item" (i.e. the address was identified to be the LRU entry, therefore the priority assigned at that location will be of higher priority once the new entry is written);

d) identifying a plurality of locations in the cache based on the address associated with the item, each of the identified locations having a priority associated therewith (all memory locations are examined to determine the lowest priority – col. 3, lines 23-44); and

e) selectively storing the item in a location of the plurality of locations selected based on a relative priority of the priority obtained for the item and the priorities associated with the plurality of locations (col. 3, lines 23-44 – the newest entry is stored in the location from which the lowest priority item was recently purged).

Despite teaching assigning priorities to addresses within the cache, Zangenehpour fails to specifically teach the use of a data table to maintain this information, (rather it is encoded in the cache itself).

Abe however teaches a computer with a cache controller and cache memory with a priority table and priority levels which stores a priority table, used to record priorities of cache addresses in a control register (Fig. 5, elements 14 and 16 – col. 3, line 36 through col. 4, line 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Zangenehpour to further include Abe's computer system into his own computer system using an LRU process for cache replacement. By doing so,

Zangenehpour could improve the speed of his cache by retaining data within the cache based on its access frequency as taught by Abe in col. 1, lines 19-42.

As for claim 32, Zangenehpour further teaches storing the item when the priority obtained for the item is higher than the priority associated with each of the plurality of locations (again, the new entry is assigned the highest priority, and the address of the cache containing the lowest priority is replaced)

As for claims 34 and 35, Zangenehpour further teaches selecting a location from a subset of the plurality of locations, the locations in the subset having a priority less than the priority obtained for the item, and the location being selected according to a replacement policy (Zangenehpour employs an LRU policy to replace the lowest priority of items with the new item to be written to the cache – col. 3 lines 22-44).

As for claims 37 and 38, Zangenehpour teaches associating the obtained priority with the location (again, each location is specifically associated with a particular location which remains intact until the entry is purged from the cache).

As for claims 17 and 18, though Zangenehpour teaches all of the elements of claim 1, he fails to specifically teach storing the priority information in a table. Additionally, he fails to teach writing the priorities of the cache to a control register.

Abe however teaches a computer with a cache controller and cache memory with a priority table and priority levels which stores a priority table, used to record priorities of cache addresses in a control register (Fig. 5, elements 14 and 16 – col. 3, line 36 through col. 4, line 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Zangenehpour to further include Abe's computer system into his own computer system using an LRU process for cache replacement. By doing so, Zangenehpour could improve the speed of his cache by retaining data within the cache based on its access frequency as taught by Abe in col. 1, lines 19-42.

6. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Zangenehpour (US Patent 5,224,217) and Abe (US Patent 5,906,000) as applied to claim 31 above, and in further view of Applicant's admitted prior art pursuant to MPEP § 2129.

As for claim 33, though the combined teachings of Zangenehpour and Abe fully disclose all the claim limitations of claim 31 (including the data table), they fail to specifically teach the data table as being a cache ability protection look aside buffer (CPLB) as recited in this claim.

Applicant however discloses that the use of such a buffer is well known in the art in paragraphs 0017-0018, all lines and in Fig. 2 (element 250) – in which Applicant correctly identified, and fully conceded it as being prior art.

MPEP § 2129 recites in part, “[w]here the specification identifies work done by another as “prior art”, the subject matter so identified is treated as admitted prior art. *In re Nomiya*, 509 F.2d 566, 571, 184 USPQ 607, 611 (CCPA 1975) (holding drawings as “prior art” to be an admission that what was pictured was prior art relative to applicant's improvement).” Continuing, the aforementioned relevant MPEP section further recites

"[c]onsequently, the examiner must determine whether the subject matter identified as "prior art" is applicant's own work, or the work of another. In the absence of another credible explanation, examiners should treat such subject matter as the work of another".

It would have been obvious to one of ordinary skill in the art at the time of the invention for the combined teachings of Zangenehpour and Abe to use a CPLB for the data table to map address and priority information for the cache. By doing so, they could exploit the well-known benefits of a CPLB including its ability to cache data in addition to storing data structures such as tables as admitted by Applicant as being well-known in the semiconductor art in paragraphs 0017-0018, all lines of Applicant's disclosure.

7. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Zangenehpour (US Patent 5,224,217) and Abe (US Patent 5,906,000) as applied to claim 31, and in further view of Tago et al. (US PG Publication 2002/0199091 A1), hereinafter Tago.

As for claim 36, though the combined teachings of Zangenehpour and Abe disclose replacing data in the cache based on an LRU policy, they fail to teach replacing the entries based on a least recently loaded policy.

Tago however teaches an apparatus for branch prediction based on history table in which he discusses cache eviction policies including LRU, FIFO (i.e. oldest or least recently loaded), and random in paragraph 0065, all lines.

It would have been obvious to one of ordinary skill in the art at the time of the invention for the combined teachings of Zangenehpour and Abe to further include Tago's apparatus into his their computer system using an LRU process for cache replacement. By doing so, they could exploit the benefits of utilizing a processor which performs its instruction branch predictions on a pattern history table, which could help to improve the prediction accuracy and minimize the amount of memory required by avoiding entry interference as taught by Tago in paragraphs 0014 through 0016, all lines.

8. Claims 2-4, and 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zangenehpour (US Patent 5,224,217) and in further view of Tago (US PG Publication 2002/0199091 A1).

As for claims 2-4, 8-9, and 10-11, Zangenehpour teaches all of the elements of these claims (per the rejection of claims 5-7, 6-7, and 6-7 respectively), including assigning priorities based on an LRU policy. Zangenehpour however teaches neither assigning priorities on a least frequently used (LFU), a least recently loaded policy, nor a pseudo random as recited in these claims.

Tago however teaches an apparatus for branch prediction based on history table in which he discusses cache eviction policies including LRU, FIFO (i.e. oldest or least recently loaded), and random in paragraph 0065, all lines.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Zangenehpour to further include Tago's apparatus into his own computer system using an LRU process for cache replacement. By doing so, Zangenehpour

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could exploit the benefits of utilizing a processor which performs its instruction branch predictions on a pattern history table, which could help to improve the prediction accuracy and minimize the amount of memory required by avoiding entry interference as taught by Tago in paragraphs 0014 through 0016, all lines.

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zangenehpour (US Patent 5,224,217) and in further view of Ozawa (US Patent 5,787,490).

As for claim 13, though Zangenehpour teaches all of the elements of claim 1, he fails to teach associating multiple processes with a priority, wherein the priority of the new item is derived from the priority of the process that generated the new item as recited in this claim.

Ozawa however teaches a multiprocess execution system that designates cache use priority based on process priority (col. 1, line 48 through col. 2, line 24 and abstract).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Zangenehpour to further include Ozawa's multiprocess execution system into his own computer system using an LRU process for cache replacement. By doing so, Zangenehpour could benefit from improved memory usage by ensuring that the highest priority process is not prevented from executing its preferential use, and further maximize process execution time as taught by Ozawa in col. 1, lines 17-45.

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10. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zangenehpour (US Patent 5,224,217) and in further view of Agarwala et al. (US Patent 6,484,237 B1), hereinafter Agarwala.

As for claims 14 and 15, Zangenehpour teaches:

a) assigning a first priority to a first portion of the plurality of memory locations (col. 3, lines 23-44 - the most recently used entry is given the highest priority);

b) assigning a second priority, lower than the first priority, to a second portion of the plurality of memory locations (col. 3, lines 23-44 - the most least used entry is given the lowest priority);

c) generating new items to store in the cache with priorities lower than or equal to the second priority (col. 3, lines 23-44 - the newest entry will be assigned a value equal to the priority of the second priority (i.e. highest)).

He fails however to teach using the first portion of the plurality of memory locations for non-cache memory location, and a digital signal processor (DSP), which uses a portion for non-caching processor operations as recited in these claims.

Agarwala however teaches a unified multilevel memory system architecture which supports both cache and addressable SRAM, which utilizes a level one unified cache for both caching and instructions (i.e. non-caching) for a DSP - col. 2, lines 55-64.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Zangenehpour to further include Agarwala's unified memory system into

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his own computer system using an LRU process for cache replacement. By doing so, Zangenehpour could improve the speed and effectiveness of his overall cache memory management by more effectively caching processor instructions and requests, as taught by Agarwala in col. 11, lines 18-49.

11. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Zangenehpour (US Patent 5,224,217) and Agarwala (US Patent 6,484,237 B1) as applied to claim 14 above, and in further view of Abe (US Patent 5,906,000).

As for claim 16, though the combined teachings of Zangenehpour and Agarwala teach all of the elements of claim 14, they fail to specifically teach writing the priorities of the cache to a control register.

Abe however teaches a computer with a cache controller and cache memory with a priority table and priority levels which stores a priority table, used to record priorities of cache addresses in a control register (Fig. 5, elements 14 and 16 – col. 3, line 36 through col. 4, line 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention for the combined teachings of Zangenehpour and Agarwala to further include Abe's computer system. By doing so, they could improve the speed of the cache by retaining data within the cache based on its access frequency as taught by Abe in col. 1, lines 19-42.

Response to Arguments

12. Applicant's arguments with respect to the prior art rejections (claims 1-18) under 35 USC §§ 102(b) and 103(a) have been fully considered, but they are not persuasive.

Under the heading Claims Rejections – 35 U.S.C. §102 (Zangenehpour), Applicant contends, "claim 1 recites 'associating a priority with the new item based on the address associated with the item.' Zangenehpour does not teach priority relating to an address associated with an item to be stored. Accordingly, Zangenehpour does not teach or suggest the claimed method"; and "the reference does not teach or suggest any step comparable to 'associating a priority with the new item based on the address associated with the item.'"

This argument however is not persuasive. First, Zangenehpour teaches (albeit not in the preferred embodiment), his method as including placing the least recently used entry of the cache to the tail of the line, and the most recently used entry of the cache at the head. In other words, data is reordered such that the priority is consistent with location (i.e. addresses) – col. 3, lines 23-44. Assuming *arguendo* that Zangenehpour does not teach this reordering of data (i.e. teaches moving the tags alone as suggested throughout the remaining portions of the reference), Zangenehpour still teaches, "priority relating to an address associated with an item to be stored" as presently recited in instant claim 1. For example (referring again to col. 3, lines 23-44), all memory locations are assigned a priority tag ranging from 0 to the total number of locations. When a replacement is made, the lowest priority is identified, and replaced first. Since the address of the item to be replaced is identified, and is assigned a

priority, the priority is associated with that new item "based on the address associated with the item" (i.e. the address was identified to contain the LRU entry, therefore the priority assigned at that location will be of higher priority once the new entry is written, and the old entry is purged)). As such, Examiner maintains Zangenehpour anticipates this limitation.

Continuing under this heading (with respect to claim 5 specifically), Applicant contends, "claim 5 recites 'otherwise not storing the new item and treating the new item as not cacheable.' No such operating condition occurs with the least recently used replacement algorithm of the reference.

Examiner maintains however that Zangenehpour does teach all the limitations of claim 5 (including this newly amended limitation), as per the rejection under 35 USC §102(b) *supra*.

Under the heading Claims Rejections – 35 U.S.C. §103, Applicant's generic argument that all claims depending on claim 1 are allowable since all remaining cited prior art fails to cure the alleged deficiencies of the Zangenehpour reference is not persuasive, as Examiner maintains that Zangenehpour anticipates claim 1 as per the arguments and rejections set forth *supra*.

Under the heading New Claims 31-38, Applicant's arguments have been fully considered, however they are moot in view of the new grounds of rejection.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Crawford et al. (US Patent 6,542,966 B1) teach a method and apparatus for managing temporal and non-temporal data in a single cache structure.

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

15. A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

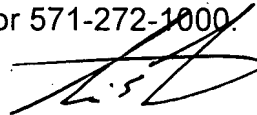
16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

17. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone

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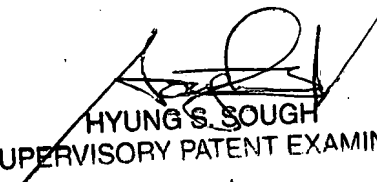
number for the organization where this application or proceeding is assigned is 571-273-8300.

18. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Craig E Walter
Examiner
Art Unit 2188

CEW



HYUNG S. SOUGH
SUPERVISORY PATENT EXAMINER
11/27/07